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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/729,254	12/05/2003	Daniel Charles Edelstein	YOR920030098US1	1156

7590 05/18/2006

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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 05/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H'A

Office Action Summary	Application No.	Applicant(s)	
	10/729,254	EDELSTEIN ET AL.	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) *2-6 and 15-42* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 7-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/729254 Attorney's Docket #: YOR920030098US1
Filing Date: 12/5/2003;

Applicant: Edelstein et al.

Examiner: Alexander Williams

Applicant's election of Species 1(a), figure 2A, claims 1, 7 and 8-14, filed 3/2/06 has been acknowledged.

This application contains claims 2-6 and 15-42 drawn to an invention non-elected without traverse.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 7-10 and 12 are rejected under 35 U.S.C. § 102(e) as being anticipated by Yamada et al. (U.S. Patent # 6,693,358 B2).

1. Yamada et al. (figures 1 to 59c) specifically figure 36 show a semiconductor carrier structure comprising: a semiconductor substrate **106** comprising a substrate material having a first coefficient of thermal expansion and a first elastic modulus; at least one through-via **108** in said semiconductor substrate, wherein each of said through-vias is filled with a conductive structure **114** having a second coefficient of thermal expansion which is less than or substantially the same as the first

8. The semiconductor carrier structure of Claim 7 wherein coefficient of thermal expansion and a second elastic modulus which is less than or equal to the first elastic modulus.

7. The semiconductor carrier structure of Claim 1, Yamada et al. show *wherein* said each conductive structure comprises a first conductive via material disposed in annular shape along the sidewalls of said through-via and having a core structure **(middle portion of 106)** comprising a second via material **(135,middle portion of 106 or 127)**.

8. The semiconductor carrier structure of claim 7, Yamada et al. show wherein said second via material comprises an insulating material **127**.

9. The semiconductor carrier structure of Claim 7, Yamada et al. show wherein said second via material comprises a conducting material **135**.

10. The semiconductor carrier structure of Claim 7, Yamada et al. show wherein said second via material comprises said substrate material **(middle portion of 106)**.

12. The semiconductor carrier structure of Claim 7, Yamada et al. show wherein said second via material comprises a material having a third coefficient of thermal expansion which is less than or about equal to said first coefficient of thermal expansion.

Claims 1, 7, 9, 11, 12 and 14 are rejected under 35 U.S.C. § 102(b) as being anticipated by Beasom et al. (U.S. Patent # 5,780,311).

1. Beasom et al. (figures 1 to 12) specifically figure 7e show a semiconductor carrier structure comprising: a semiconductor substrate **((ISLAND)** comprising a substrate material having a first coefficient of thermal expansion and a first elastic modulus; at least one through-via in said semiconductor substrate, wherein each of said through-vias is filled with

a conductive structure **(POLY)** having a second coefficient of thermal expansion which is less than or substantially the same as the first coefficient of thermal expansion and a second elastic modulus which is less than or equal to the first elastic modulus.

7. The semiconductor carrier structure of Claim 1, Yamada et al. show *wherein* said each conductive structure comprises a first conductive via material disposed in annular shape along the sidewalls of said through-via and having a core structure **(POLY)** comprising a second via material.

9. The semiconductor carrier structure of Claim 7, Beasom et al. show wherein said second via material comprises a conducting material **(POLY)**.

11. The semiconductor carrier structure of Claim 7, Beasom et al. show wherein said second via material is selected from the group consisting of **polyimide**, thermid, KJ, photosensitive **polyimide**, SiLK, or other high-temperature polymer.

12. The semiconductor carrier structure of Claim 7, Beasom et al. show wherein said second via material comprises a material having a third coefficient of thermal expansion which is less than or about equal to said first coefficient of thermal expansion.

14. The semiconductor carrier structure of Claim 7, Beasom et al. show wherein said second via material comprises of silica or a silicate glass-filled high temperature polymer **(POLY)**.

Claims 1, 7, 9 and 12-14 are rejected under 35 U.S.C. § 102(e) as being anticipated by Kodama et al. (U.S. Patent # 6,700,175 B1).

1. Kodama et al. (figures 1 to 34) specifically figures 9 and 10 show a semiconductor carrier structure comprising: a semiconductor substrate **43,42** comprising a substrate material having a first coefficient of thermal expansion and a first elastic modulus; at least one through-via in said semiconductor substrate, wherein each of said through-vias **46** is filled with a conductive structure **50,55** having a second coefficient of thermal expansion which is less than or substantially the same as the first coefficient of thermal expansion and a second elastic modulus which is less than or equal to the first elastic modulus.

7. The semiconductor carrier structure of Claim 1, Kodama et al. show *wherein* said each conductive structure comprises a first conductive via **50** material disposed in annular shape along the sidewalls of said through-via and having a core structure comprising a second via material **55**.

9. The semiconductor carrier structure of Claim 7, Kodama et al. show wherein said second via material comprises a conducting material.

12. The semiconductor carrier structure of Claim 7, Kodama et al. show wherein said second via material comprises a material having a third coefficient of thermal expansion which is less than or about equal to said first coefficient of thermal expansion.

13. The semiconductor carrier structure of Claim 7, Kodama et al. show wherein said second via material comprises silicate glass ***55***.

14. The semiconductor carrier structure of Claim 7, Kodama et al. wherein said second via material comprises of silica or a silicate glass-filled high temperature polymer.

(37) The second trench 46 is formed in the p.sup.- -type silicon layer 43 by isotropically etching the p.sup.- -type silicon layer 43 using a silicon oxide film as a mask. The depth d3 of the second trench 46 is 0.5 .mu.m to 10 .mu.m. The first trench 52 is formed in the p.sup.- -type silicon layer 43 by anisotropically etching the p.sup.- -type silicon layer 43 using the same mask. The depth d4 of the first trench 52 is 1 .mu.m to 100 .mu.m. The width w4 of the first trench 52 is 0.1 .mu.m to 10 .mu.m. A silicon oxide film is formed on the sides of the second trench 46 and the first trench 52 by thermal oxidation. The silicon oxide film formed on the side of the second trench 46 becomes the gate oxide film 48. The silicon oxide film formed on the side of the first trench 52 becomes the silicon oxide film 53.

(38) For example, the PSG film 55 is formed by CVD so as to cover the p.sup.--type silicon layer 43. The PSG film 55 is annealed at a temperature of 800.degree. C. to 900.degree. C. for 10 min to 300 min, for example. This causes the PSG film 55 to reflow and buried in the first trench 52, as shown in FIG. 12. Since the silicon oxide film 53 functions as a diffusion barrier, diffusion of n-type impurities into the p.sup.- -type silicon layer 43 can be prevented.

(39) The n-type impurities contained in the PSG film 55 are diffused into the p.sup.- -type silicon layer 43 by solid phase diffusion through the sidewall of the first trench 52, thereby forming the n.sup.- -type semiconductor regions 41 in the p.sup.- -type silicon layer 43 near the first trench 52. The diffusion
conditions are as follows.

(40) Diffusion source: PSG

(41) Diffusion temperature: 900.degree. C. to 1100.degree. C.

(42) Diffusion time: 1 min to 300 min

(43) Regions of the p.sup.- -type silicon layer 43 in which the n-type impurities are not diffused become the p.sup.- -type semiconductor regions 42. A structural section in which the p.sup.- -type semiconductor regions 42 and the n.sup.- -type semiconductor regions 41 are arranged alternately is thus formed in the p.sup.- -type silicon layer 43.

(44) A polysilicon film is formed by CVD so that the second trench 46 is filled therewith, as shown in FIG. 14. The gate electrode 50 is formed by patterning this polysilicon film. Using a resist as a mask, n-type impurities such as phosphorus ions are implanted into the p.sup.- -type silicon layer 43 thereby forming the source regions 54, as shown in FIG. 9. The vertical semiconductor device 40 is completed in this manner.

(45) Description of Effect

(46) According to the third embodiment, the n.sup.- -type semiconductor regions 41 are formed by diffusing the n-type impurities contained in the PSG film 55 into the p.sup.- -type silicon layer 43 by solid phase diffusion through the sidewall of the first trench 52, as shown in FIG. 13. Therefore, the n.sup.- -type semiconductor regions 41 can be formed without filling the first trenches 52 by epitaxial growth. This enables the degree of integration of the vertical semiconductor device 40 to be increased.

Claim 1 is rejected under 35 U.S.C. § 102(e) as being anticipated by Matsuo et al. (U.S. Patent # 6,933,205 B2).

1. Matsuo et al. (figures 1 to 22B) specifically figure 5 show a semiconductor carrier structure comprising: a semiconductor substrate **41** comprising a substrate material having a first coefficient of thermal expansion and a first elastic modulus; at least one through-via **45** in said semiconductor substrate, wherein each of said through-vias is filled with a conductive structure **47** having a second coefficient of thermal expansion which is less than or substantially the same as the first coefficient of thermal expansion and a second elastic modulus which is less than or equal to the first elastic modulus.

Initially, it is noted that the 35 U.S.C. § 103 rejection based on a conductive structure and a second via material deals with an issue (i.e., the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured as a single unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

In re Fridolph 135 USPQ 319 (CCPA 1962) deals with submitted affidavits relating to this issue. The underlying issue in In re Fridolph was related to the end result of making a multi-piece structure into a one-piece structure. Generally, favorable patentable weight was accorded if the one-piece structure yielded results not expected from the modification of the two-piece structure into a single piece structure.

Claims 7 and 9 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Matsuo et al. (U.S. Patent # 6,933,205 B2).

7. The semiconductor carrier structure of Claim 1, Matsuo et al. show *wherein* said each conductive structure comprises a first conductive via material disposed in annular shape along the sidewalls of said through-via and having a core structure comprising a second via material.

9. The semiconductor carrier structure of Claim 7, Mausuo et al. show wherein said second via material comprises a conducting material.

Therefore, it would have been obvious to one of ordinary skill in the art to use the conductive structure and the second via material as "merely a matter of obvious engineering choice" as set forth in the above case law.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/774,680,773,700,698,701,758,489,329,339,302,328,e23.006,e23.172,e23.174,e23.004,e23.011,e27.046,e23.011,e25.013,e23.067,e23.007	5/14/06
Other Documentation: foreign patents and literature in 257/774,680,773,700,698,701,758,489,329,339,302,328,e23.006,e23.172,e23.174,e23.004,e23.011,e27.046,e23.011,e25.013,e23.067,e23.007	5/14/06
Electronic data base(s): U.S. Patents EAST	5/14/06

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
5/14/06